

Figure 1

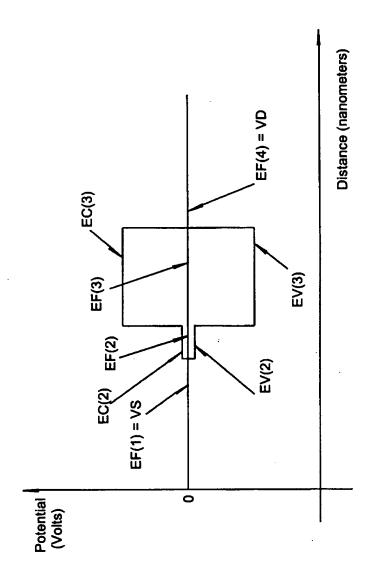


Figure 2a

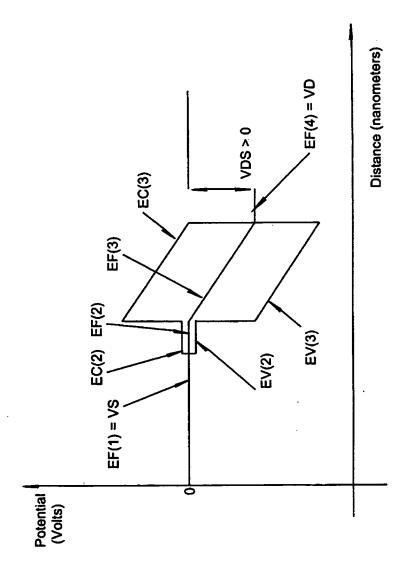


Figure 2b

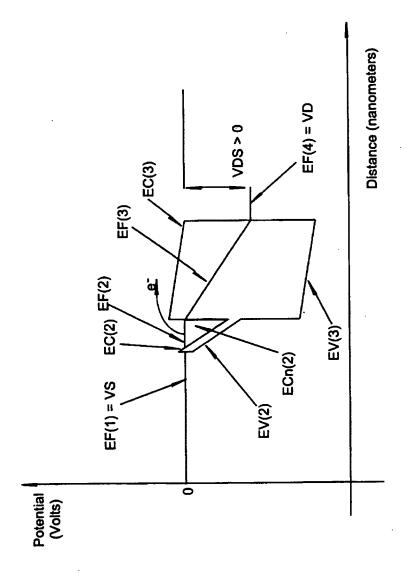


Figure 2c

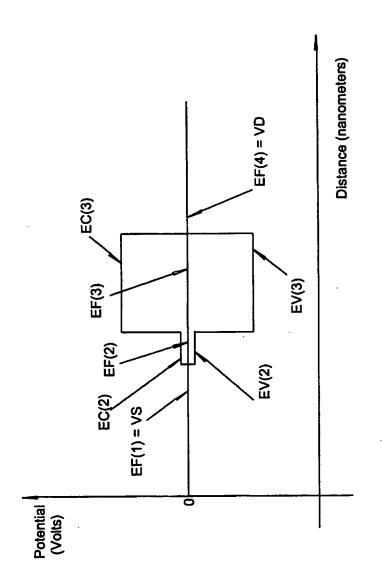


Figure 3a

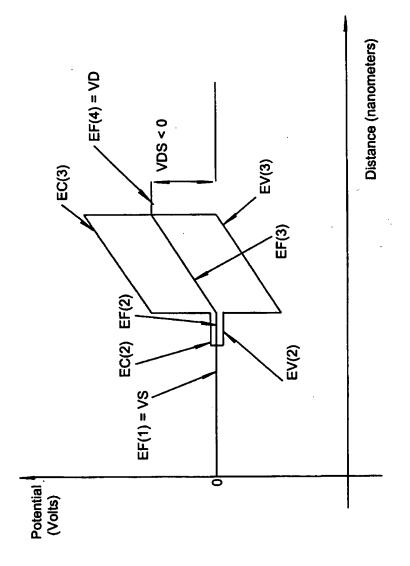


Figure 3b

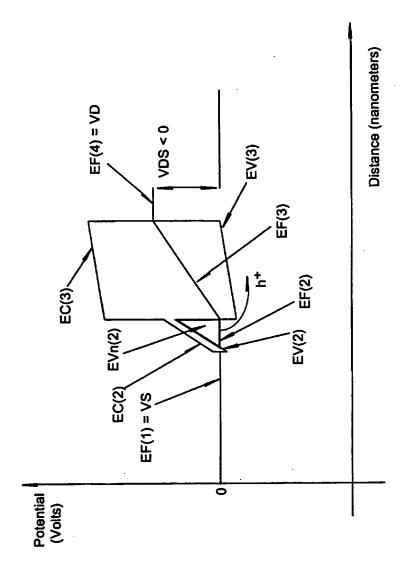
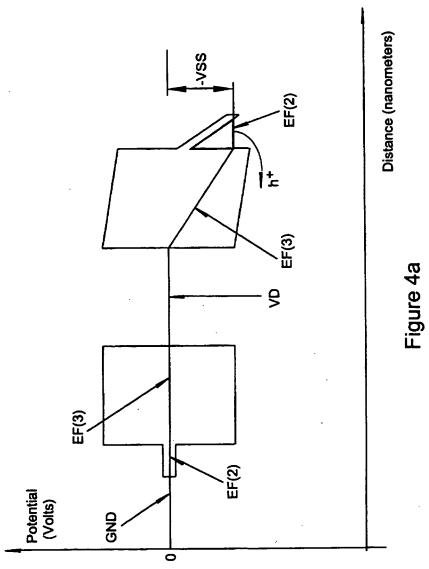


Figure 3c



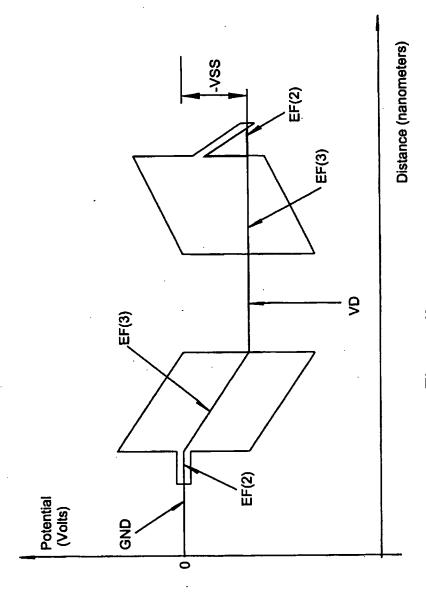


Figure 4b

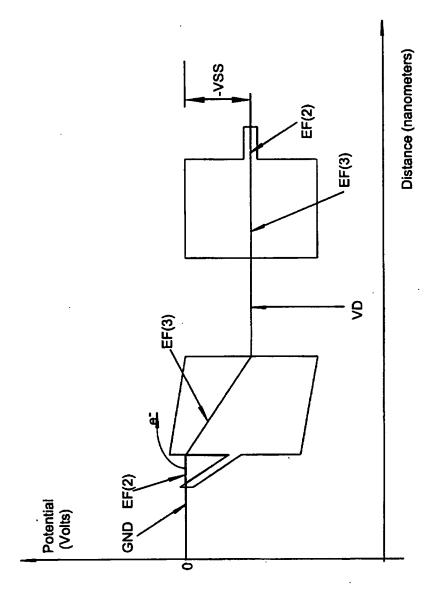


Figure 4c

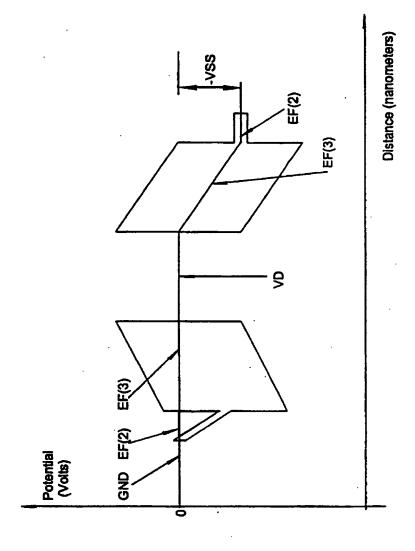


Figure 4d

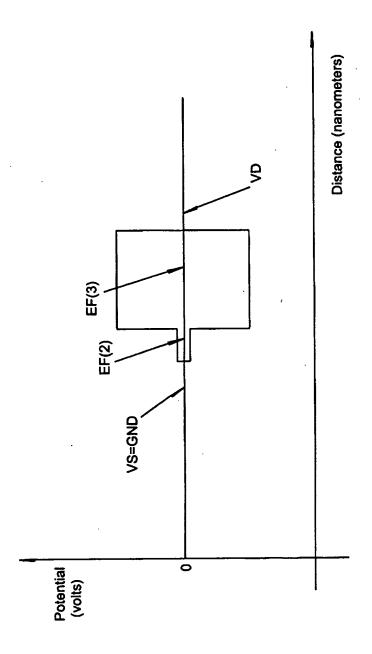


Figure 5a

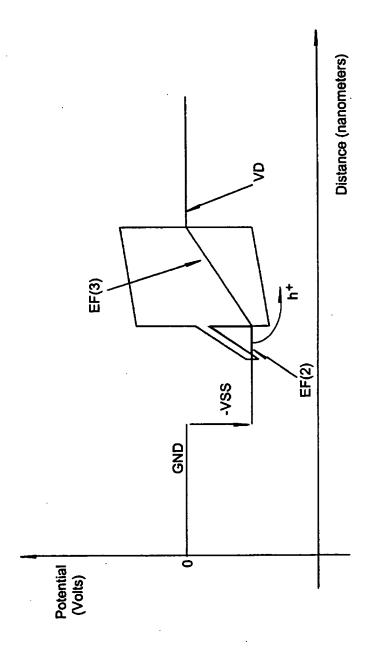


Figure 5b

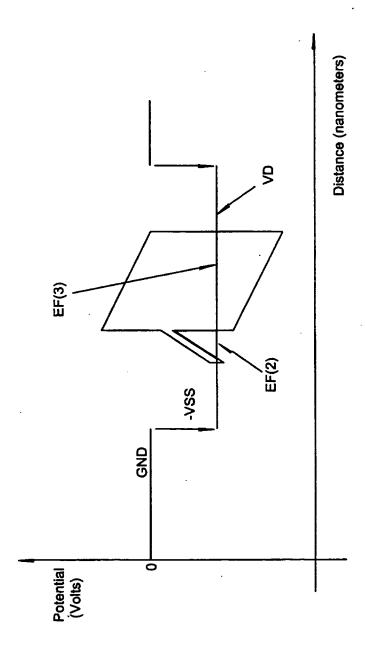


Figure 5c

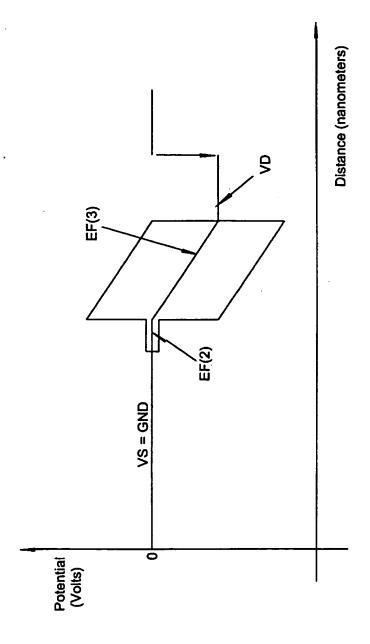


Figure 5d

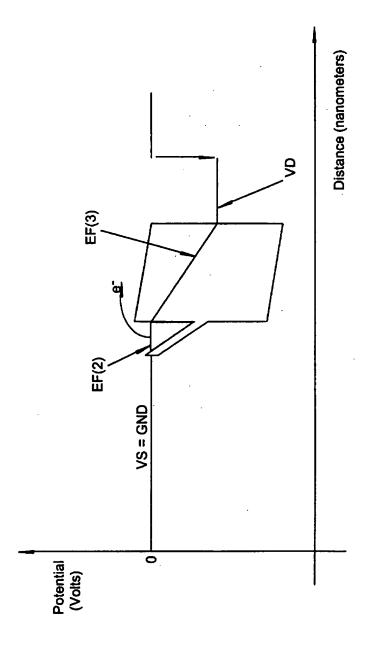


Figure 5e

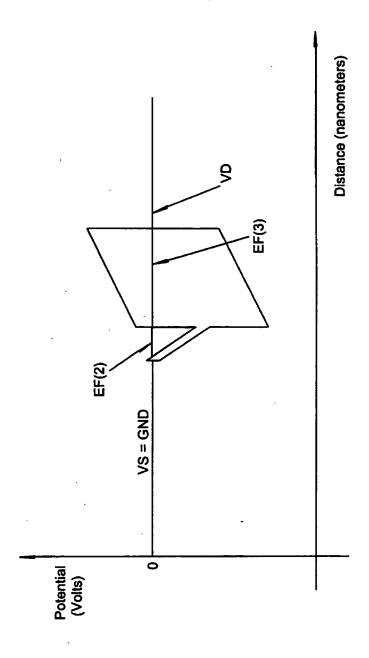


Figure 5f

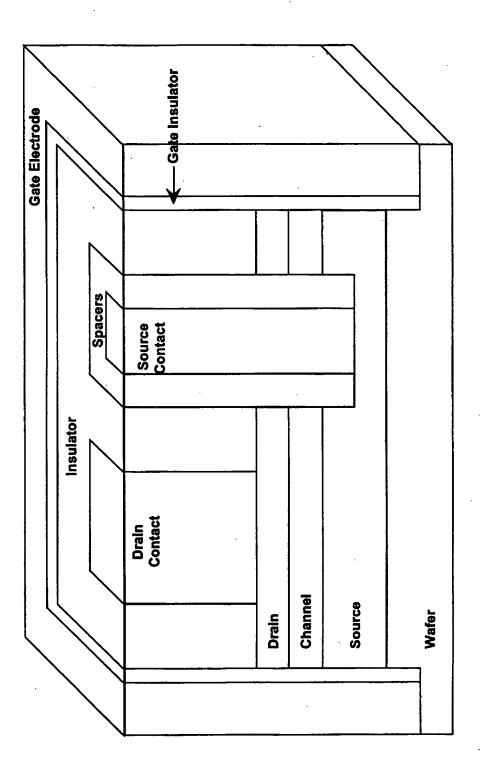


Figure 6

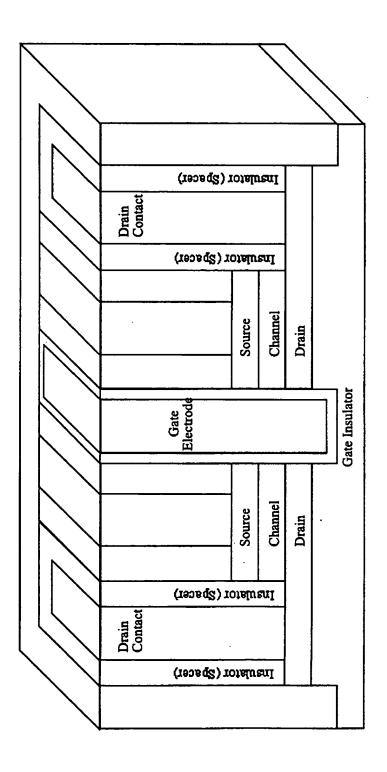


Figure 7a

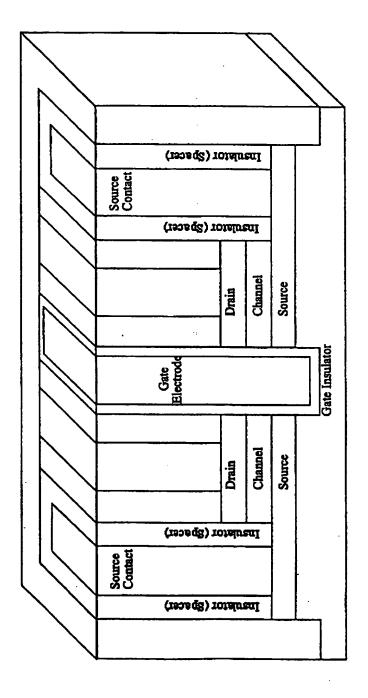


Figure 7b

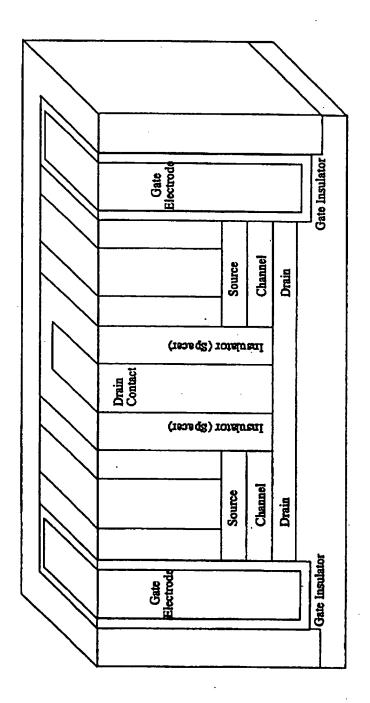


Figure 7c

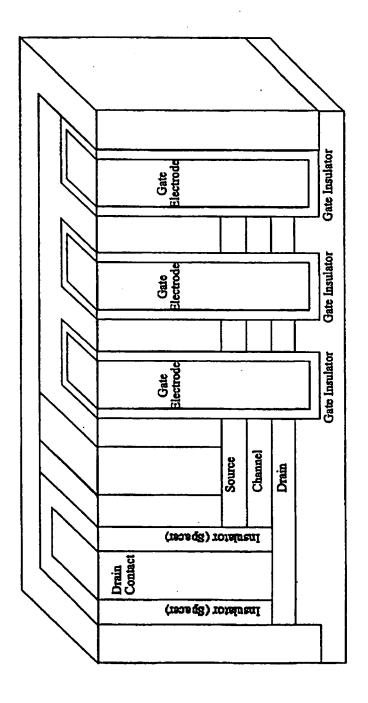


Figure 8

Figure 9: 4-Input CMOS "NOR" Logic Gates

	Gate	
	Gate	
	Source Gate Gate	
) regions	Gate	
Isolation (SiO2) regions	Source	
<u>*</u>	Drain	
	Source 9 layers	
	iate Gate Source K (Si3N4) over device layers	
	Gate	
	Gate	

Figur 9a: Static Source Voltage Supply (separate "NMOS" and "PMOS"

	Drain	
	Source] [2]
Isolation (SiO2) regions	Gate	Hardmask (Si3N4) over device layers
(SiO2)	6	ر مر
olation	Gate	Si3N4)
15	[·	nask (
	Gate	Hard
		_
	Gate	

Figure 9b: Dynamic Source Voltage Supply (single device as "NMOS" and "PMOS")

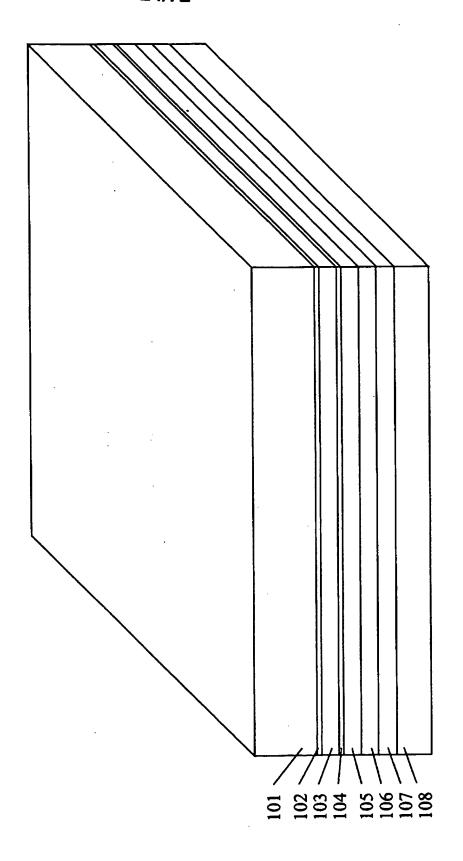


Figure 10A

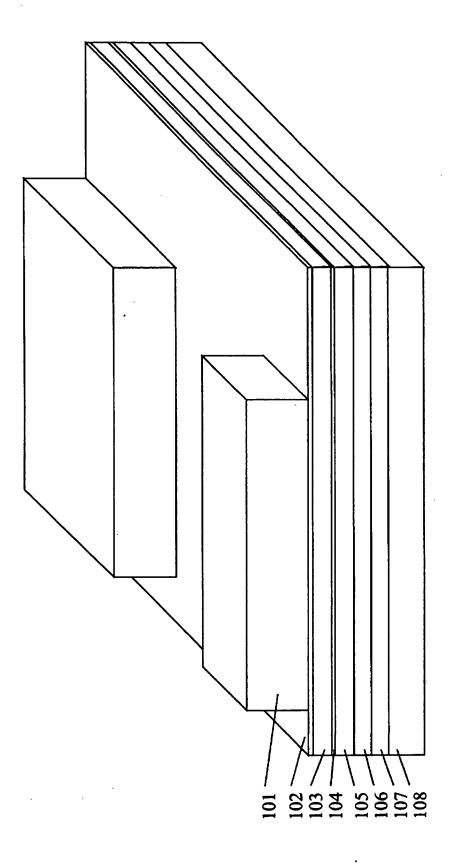


Figure 10B

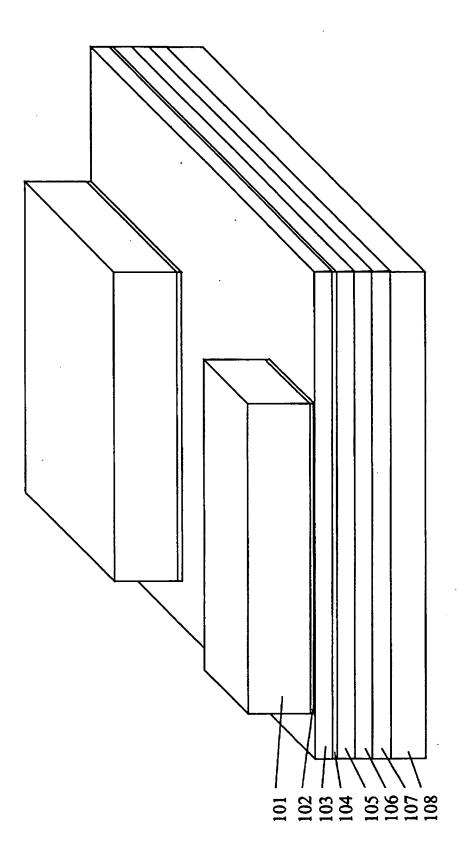


Figure 10C

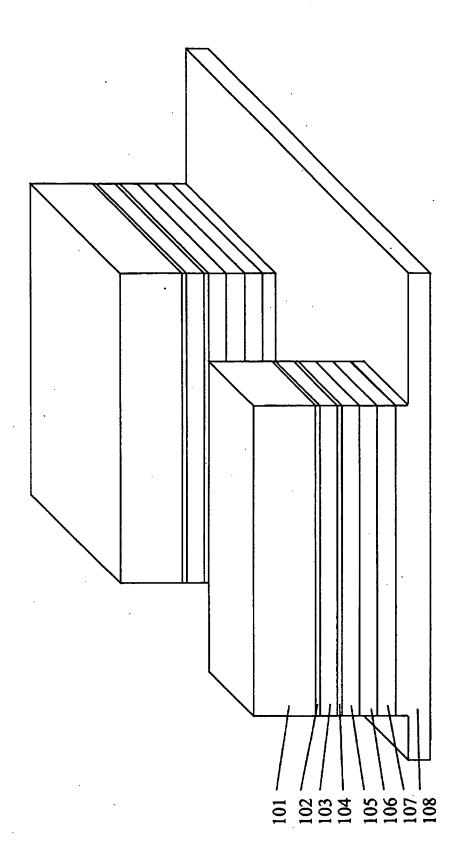


Figure 10D

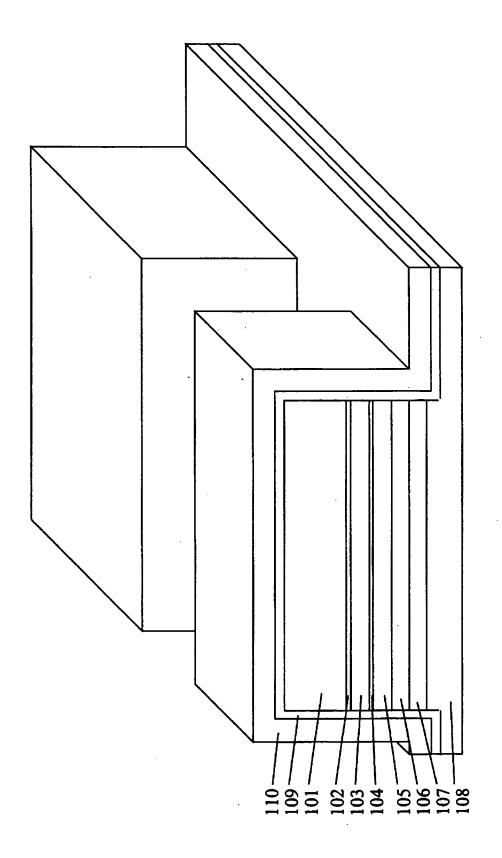


Figure 10E

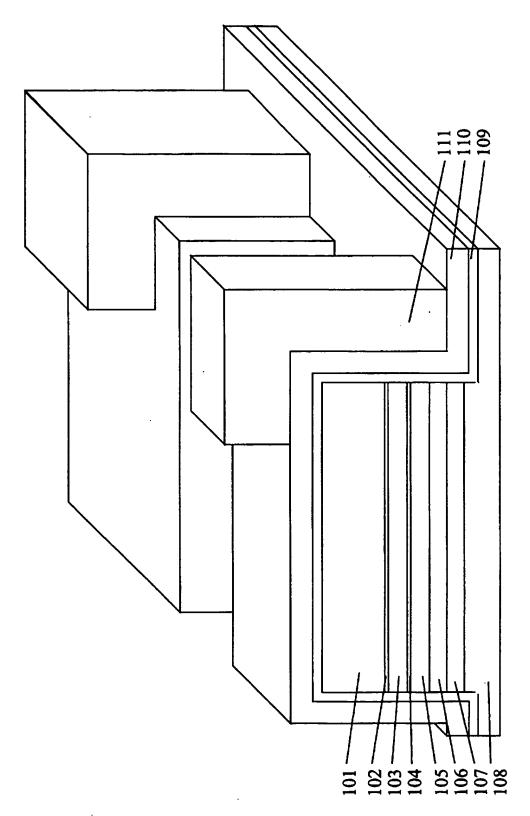


Figure 10F

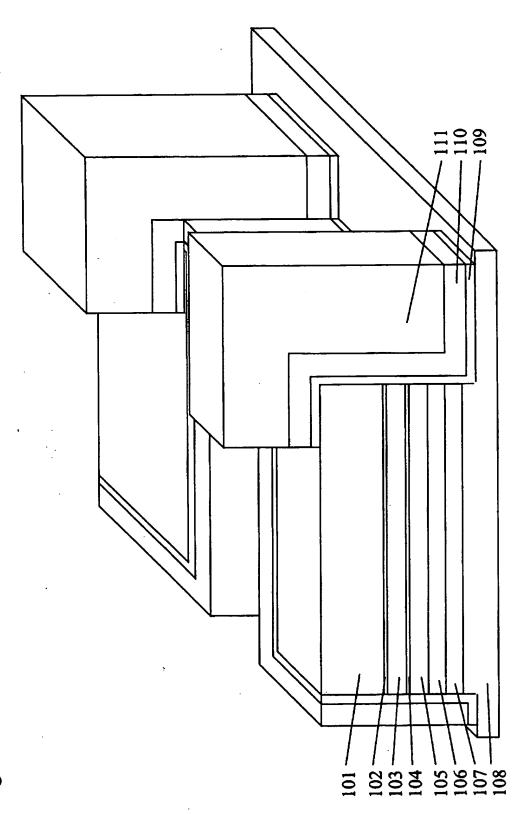


Figure 10G

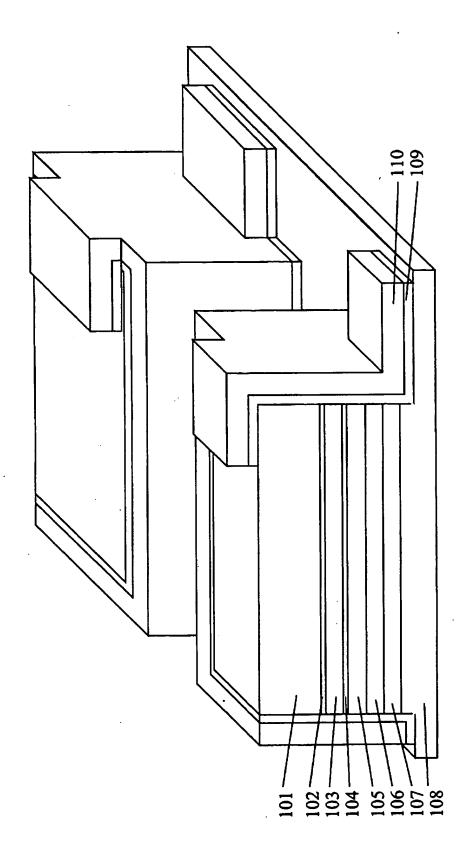


Figure 10H

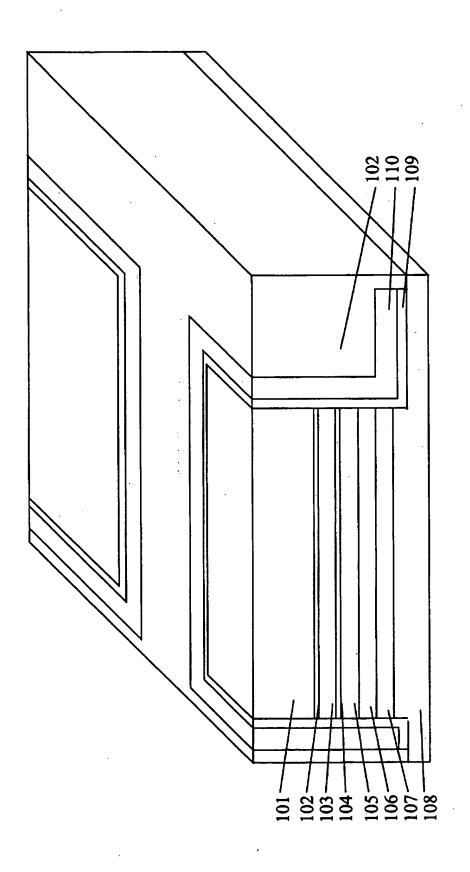


Figure 10I

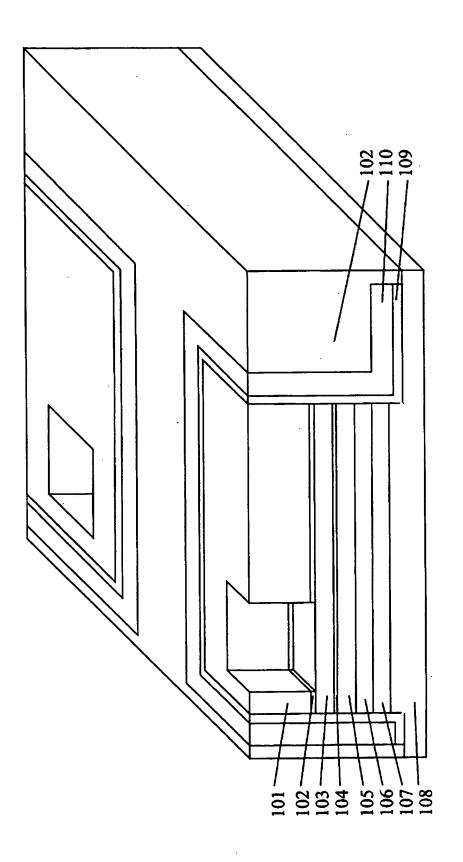


Figure 101

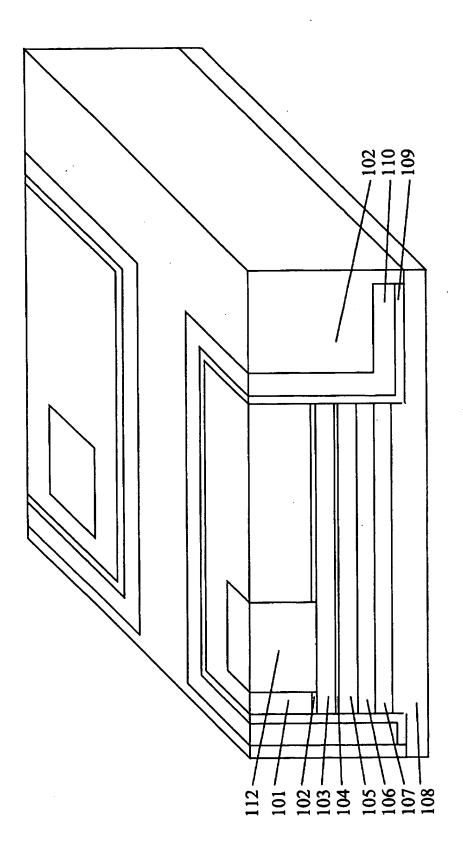


Figure 10K

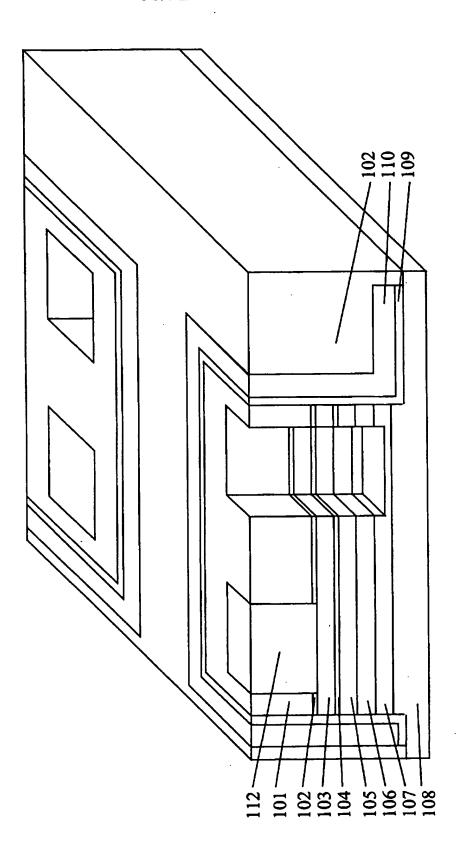


Figure 10L

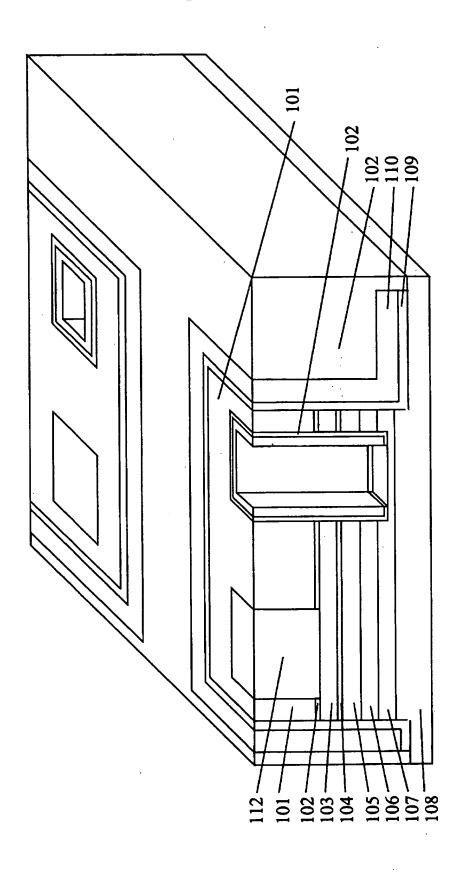


Figure 10M

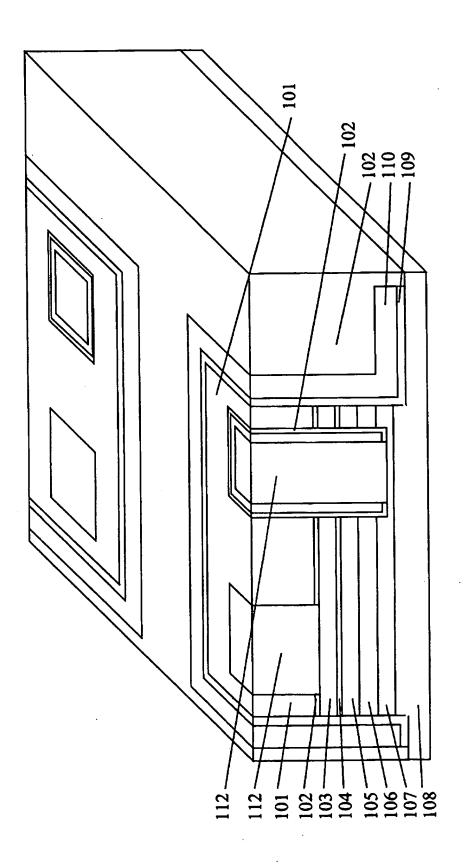


Figure 10N

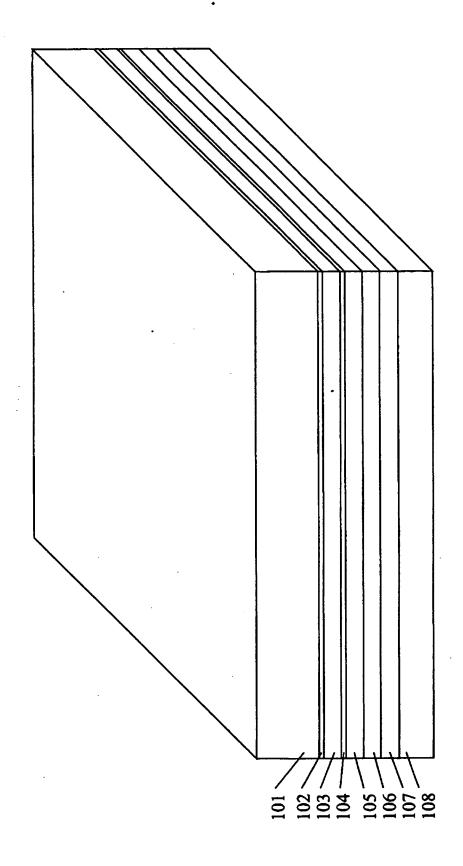


Figure 11A

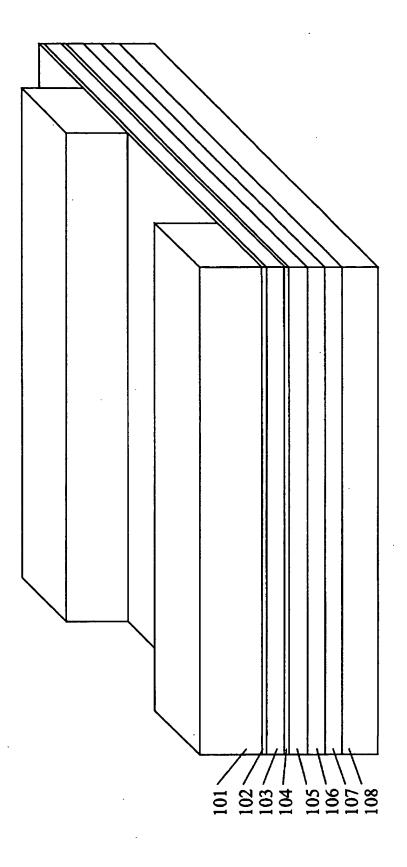


Figure 11B

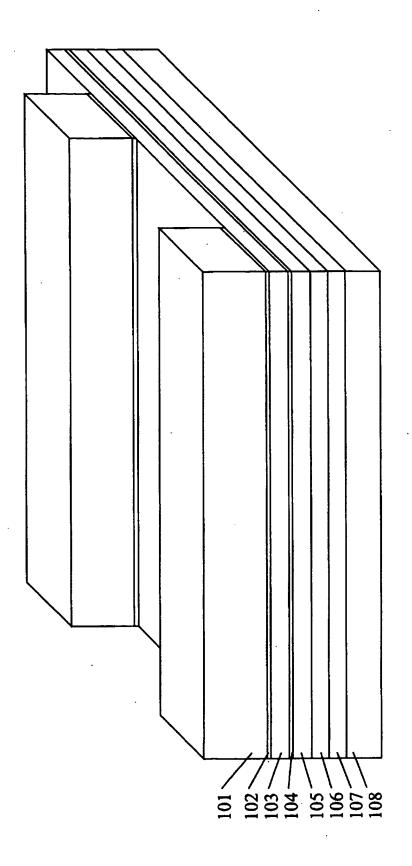


Figure 11C

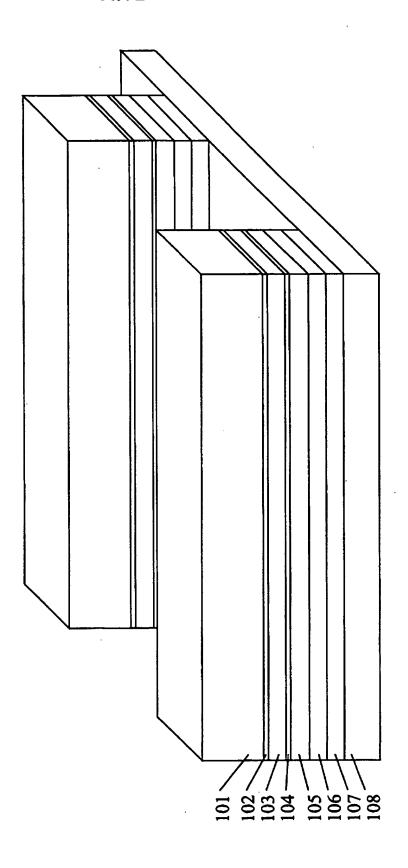


Figure 11D

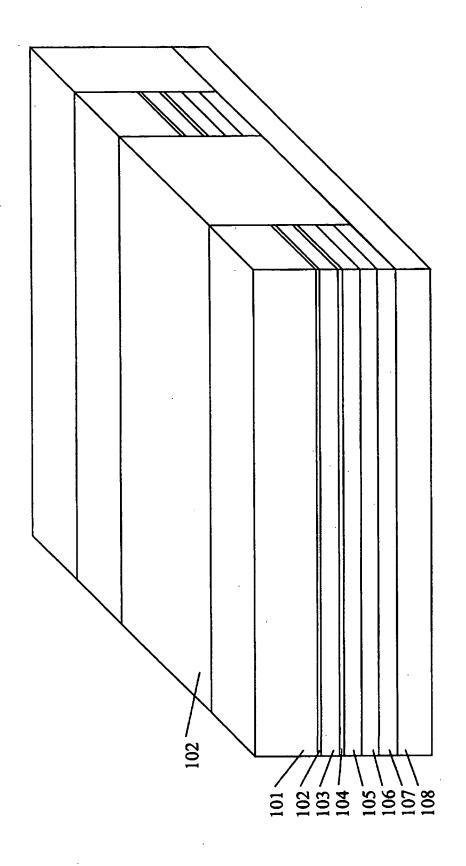


Figure 11E

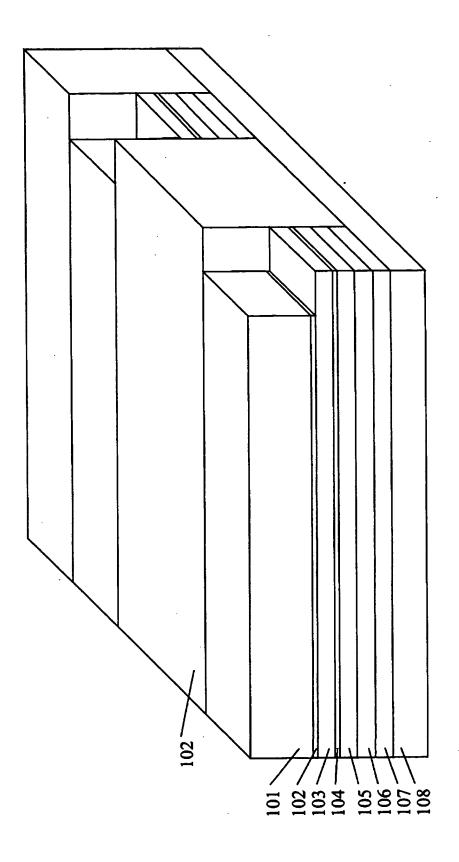


Figure 11F

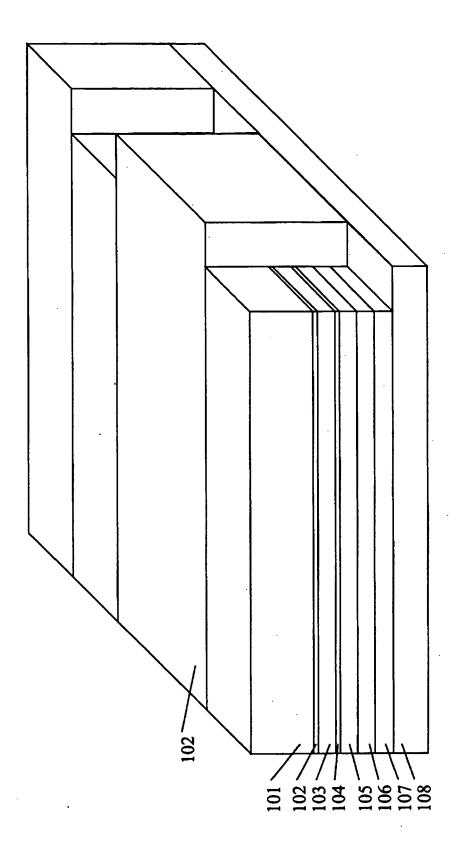


Figure 11G

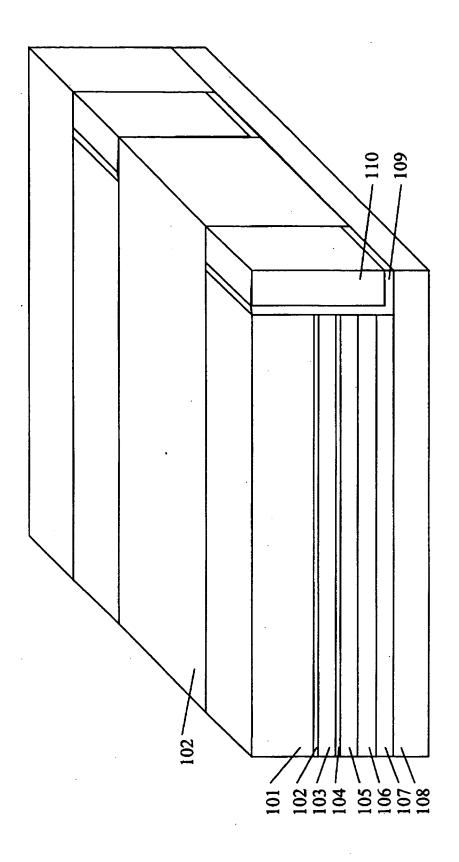


Figure 11H

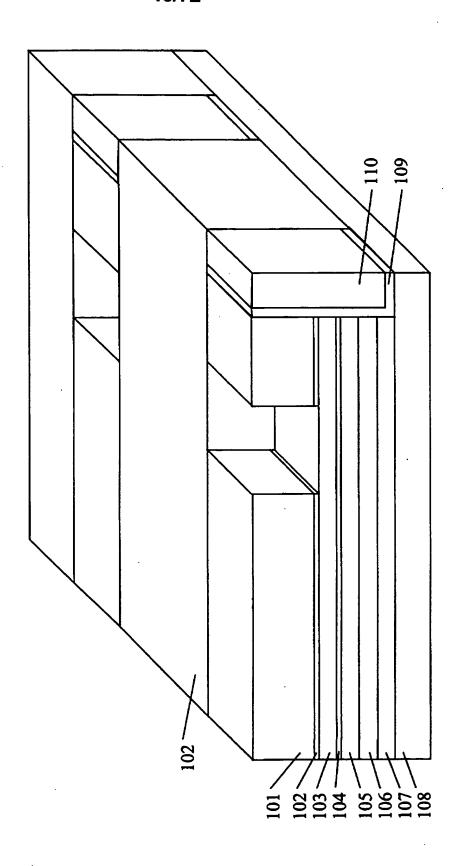


Figure 111

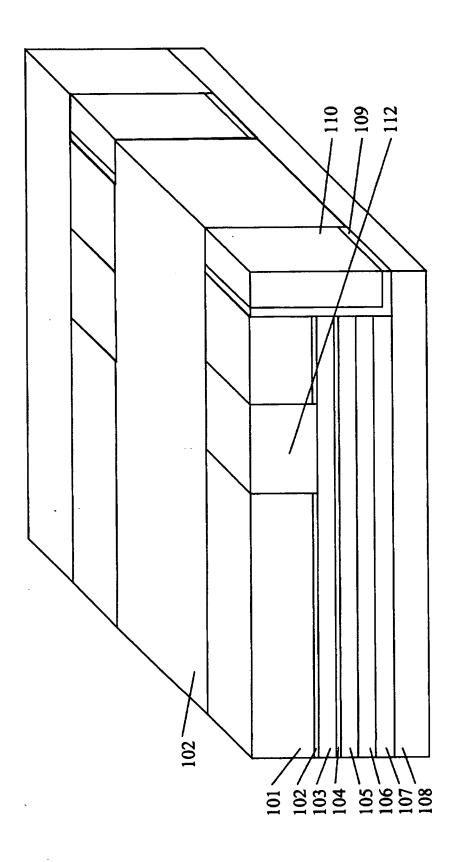


Figure 11J

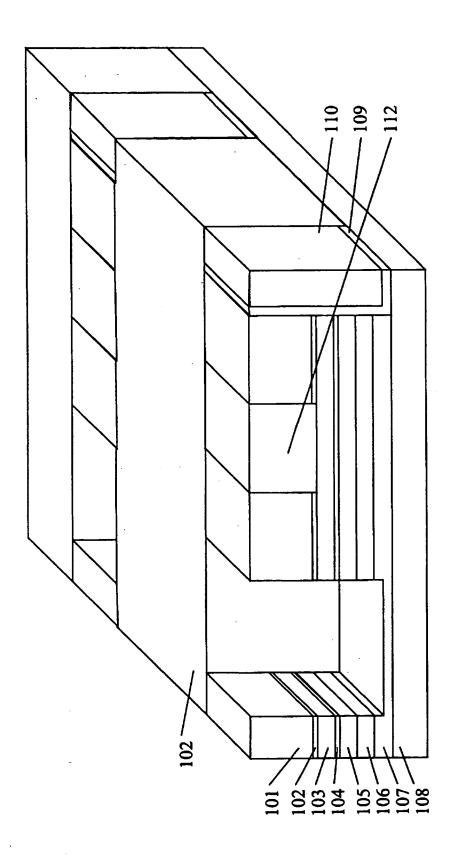


Figure 11K

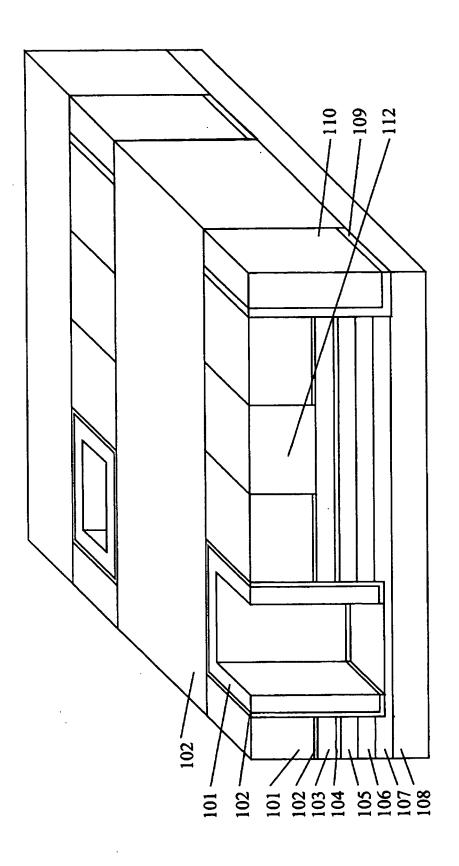


Figure 11L

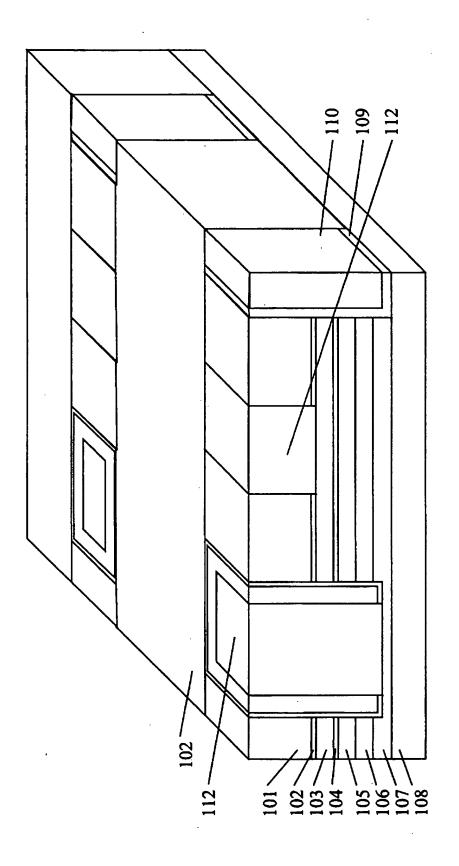


Figure 11M

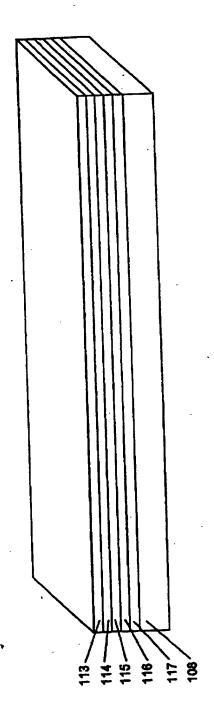


Figure 12.

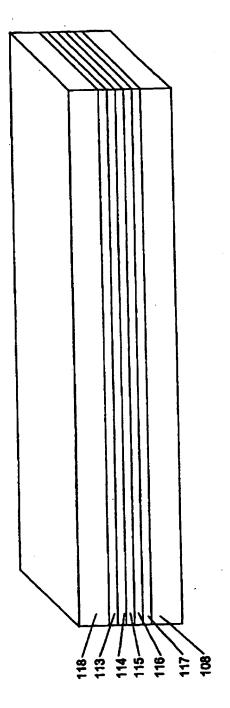


Figure 12

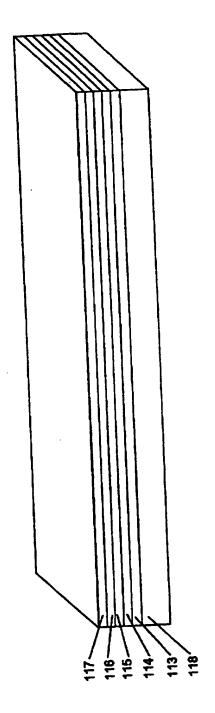


Figure 12C

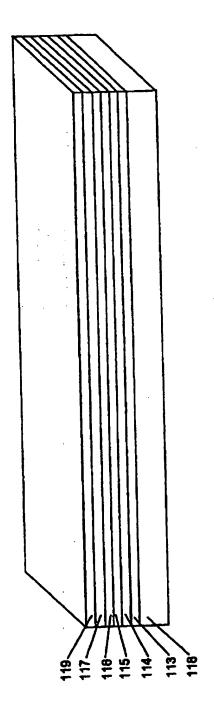


Figure 12D

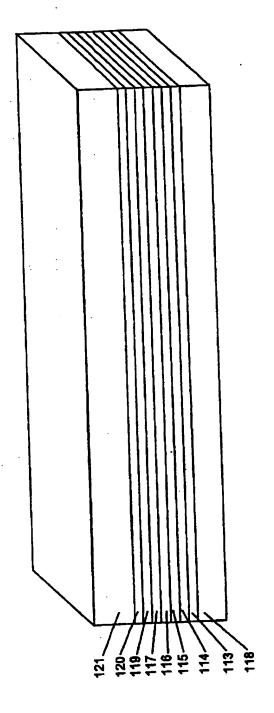


Figure 12E

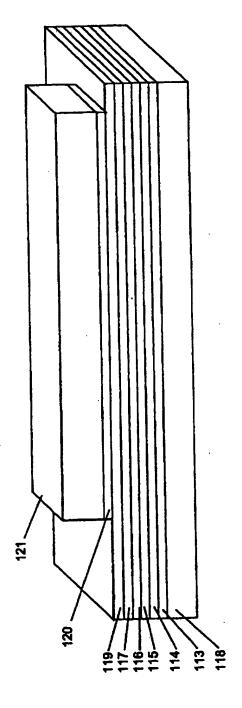


Figure 12

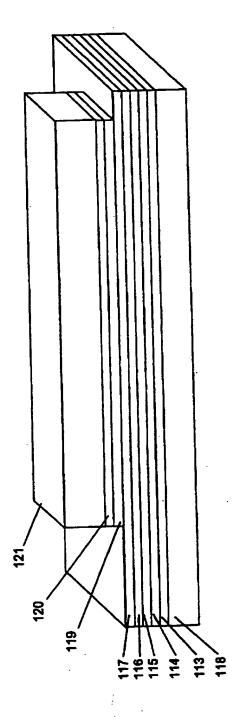


Figure 12G

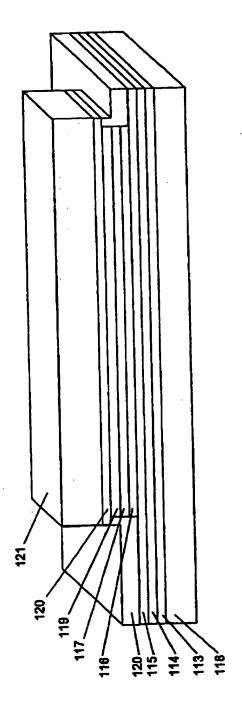


Figure 12

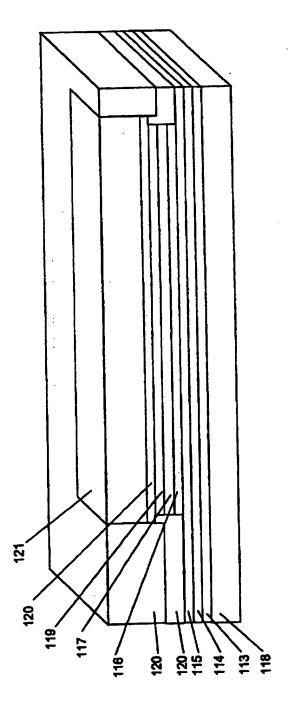


Figure 12I

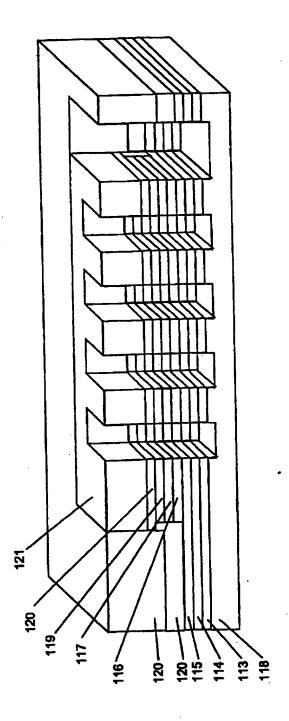


Figure 12

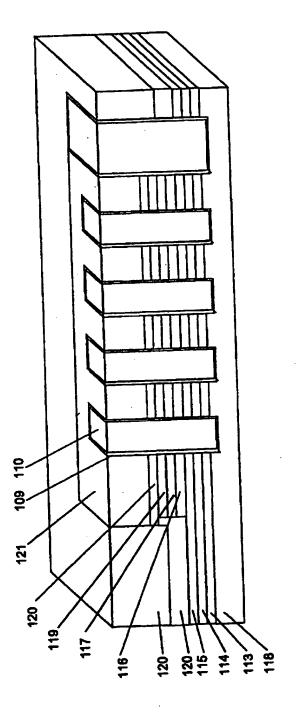


Figure 12

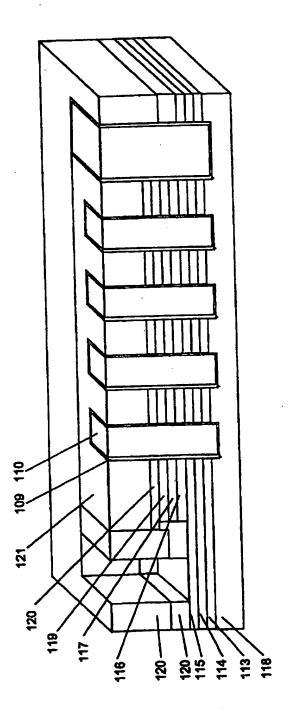


Figure 12

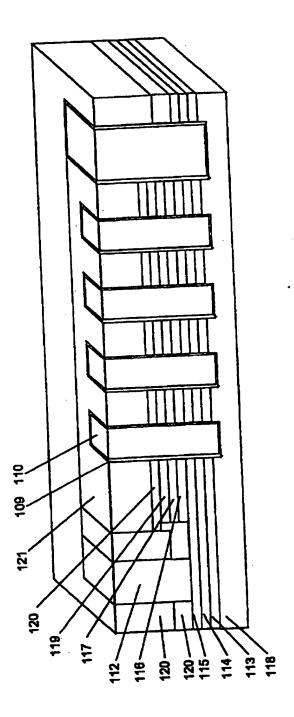


Figure 12M

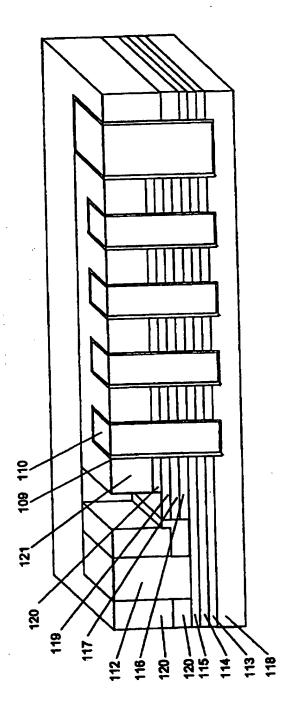


Figure 12N

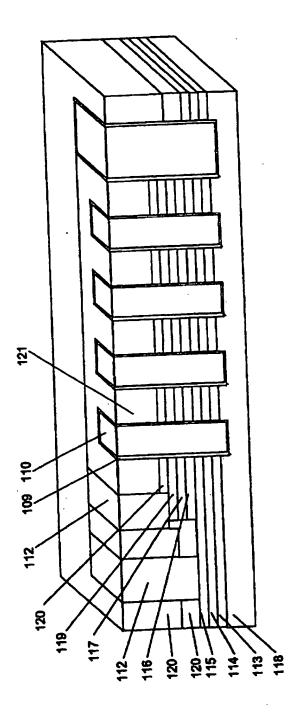


Figure 120

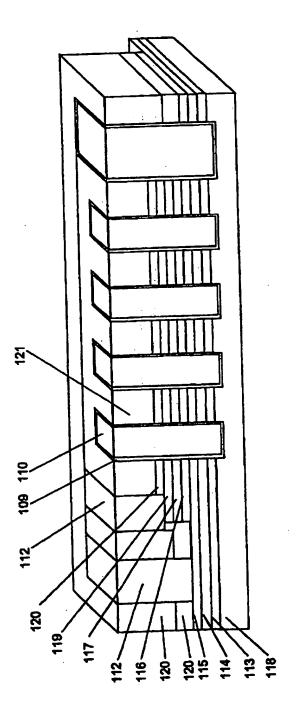


Figure 12

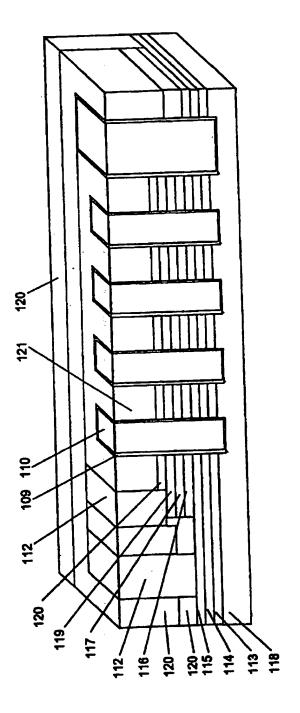


Figure 12Q

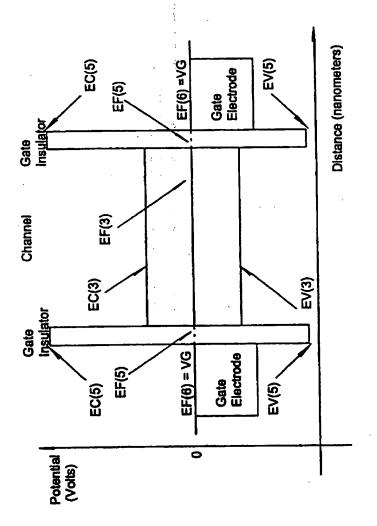


Figure 13a

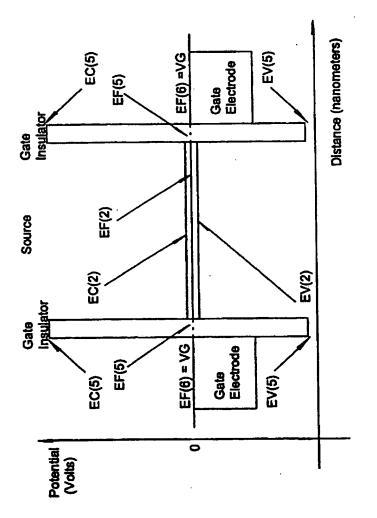


Figure 13b

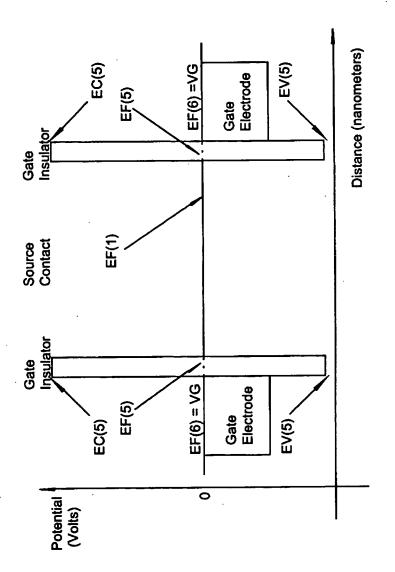


Figure 13c

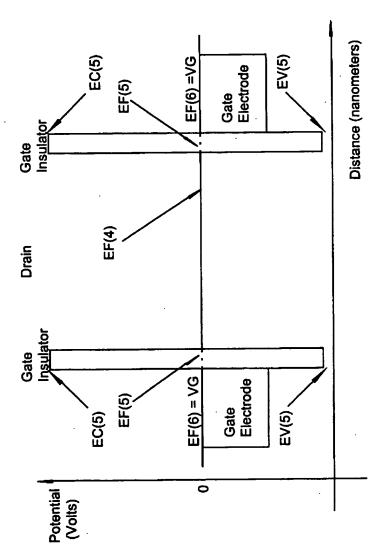


Figure 13d

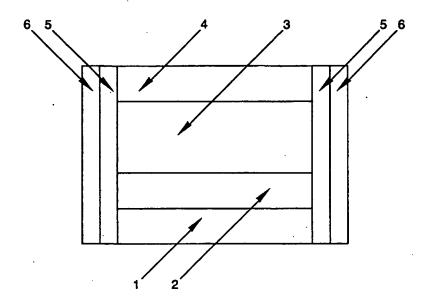


Figure 14

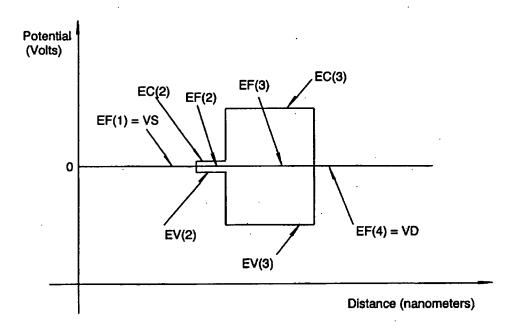


Figure 15